

**INFORMATION DISCLOSURE  
CITATION IN AN  
APPLICATION**

ATTY. DOCKET NO.  
**43876-153**

SERIAL NO.  
**Continuation of S rial  
No. 10/646,787**

APPLICANT  
**HANSEN, et al.**

FILING DATE  
**January 16, 2004**

GROUP  
**To be assigned**

(PTO-1449)

**U.S. PATENT DOCUMENTS**

EXAMINER'S INITIALS	PATENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE
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	4,489,393	12/18/84	Kawahara, et al.			
	4,701,875	10/20/87	Konishi, et al.			
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	4,956,801	09/11/90	Priem et al.			
	4,969,118	11/06/90	Montoye, et al.			
	4,975,868	12/04/90	Freerksen			
	5,032,865	07/16/91	Schlunt			
	5,157,388	10/20/92	Kohn			
	5,201,056	04/06/93	Daniel, et al.			
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Parallel Computers for Graphics Applications, Adam Levinthal, Pat Hanrahan, Mike Paquette, Jim Lawson, Pixar San Rafael, California, 1987

Organization of the Motorola 88110 Superscalar RISC Microprocessor, Keith Diefendorff and Michael Allen, 1992

Microprocessor Report, Volume 7 Number 13, October 4, 1993, IBM Regains Performance Lead with Power2, Six Way Superscalar CPU in MCM Achieves 126 SPECint92.

IBM Creates PowerPC Processors for AS/400, Two New CPU's Implement 64-Bit Power PC with Extensions by Linley Gwennap, July 31, 1995.

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	5,408,581	04/18/95	Suzuki, et al.			
	5,423,051	06/06/95	Fuller, et al.			
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	Osborne McGraw-Hill, i860 <sub>m</sub> Microprocessor Architecture, Neal Margulis, Foreword by Les Kohn, 1990, 8-10, 171-175, 182-183
	A General-Purpose Array Processor for Seismic Processing, Nov-Dec., 1984, Volume 1, No. 3) Revisiting past digital signal processor technology, Don Shaver- Jan-Mar. 1998, 15th Anniversary Issue, 5-26
	Accelerating Multimedia with Enhanced Microprocessors, Ruby B. Lee, IEEE Micro., April 1995, 22-32

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	5,734,874	03/31/98	Van Hook, et al.			
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	5,802,336	09/01/98	Peleg, et al.			
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	5,922,066	07/13/99	Cho, et al.			
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EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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		US 4,814,976	03/21/1989	Craig C. Hansen, et al.	
		US 5,031,135	07/09/1991	Patel	
		US 5,280,598	01/1994	Osaki et al.	
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		US 5,768,546	06/1998	Kwon	
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## OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.
		IEEE Draft Standard for "Scalable Coherent Interface-Low-Voltage Differential Signal Specifications And Packet Encoding", IEEE Standards Department, P1596.3/D0.15 (March 1992)
		IEEE Draft Standard for "High-Bandwidth Memory Interface Based on SCI Signaling Technology (RamLink)", IEEE Standards Department, Draft 1.25 IEEE P1596.4-199X (May 1995)
		IBM, "The PowerPC Architecture: A Specification For A New Family of Risc Processors", 2nd Ed., Morgan Kaufmann Publishers, Inc., (1994).
		Hewlett-Packard Co., "PA-RISC 1.1 Architecture and Instruction Set", Manual Part No. 09740-90039, (1990).
		MIPS Computer Systems, Inc., "MIPS R4000 User's Manual", Mfg. Part No. M8-00040, (1990).

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. //J.M.//

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		US 5,819,101	10/6/1998	Alexander Peleg, et al	
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